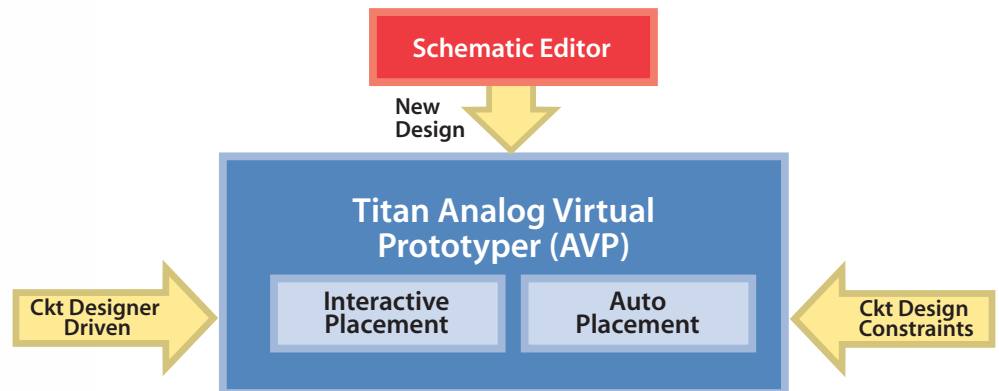


TitanTM AVP

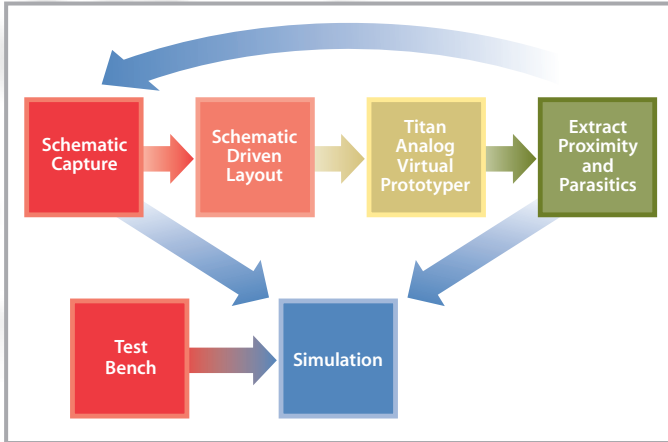
- Improves layout productivity by creating fast and accurate device-level prototypes
- Delivers best quality of results with minimal manual intervention through intelligent device placement
- Provides accelerated layout-to-schematic convergence

Titan Analog Virtual Prototyper (AVP) creates fast and accurate prototypes of the layout of analog blocks and captures layout-dependent proximity effects early in the circuit design phase, allowing designers to avoid time-consuming schematic-to-layout iterations. The same layout-dependent effects can be used in traditional simulation frameworks to ensure layout-aware simulation. Titan AVP's simple user interface provides early visibility into parasitic R and C, as well as proximity effects including STI stress, WPE, OD-OD spacing and poly- to-poly spacing. Titan AVP also includes a detailed device placement engine that produces a high-quality, DRC-clean layout. The powerful constraint-based auto placement tool can handle various placement styles including area, row and stack for a new layout.



Analog circuit design at lower geometries involves multiple iterations between the schematic and layout to address proximity effects that change with device placement. Titan AVP empowers circuit designers to create a prototype layout of analog blocks quickly. A very easy grouping/ungrouping ability provides intuitive and fast manual transistor-level placement. Analog placement constraints of matching, symmetry, alignment and spacing are captured using simple commands and intuitive shortcuts. Intricate common-centroid patterns can be entered using device modules. The proximity parameters are extracted from partial layout and are used in a layout-aware simulation flow.

Titan™ AVP



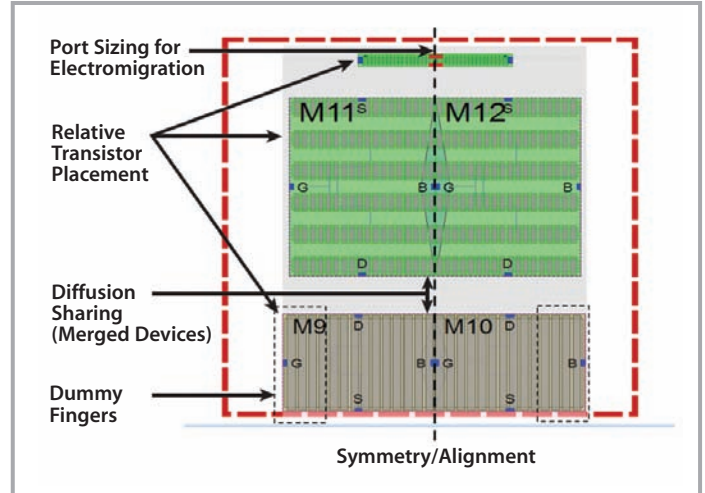
Once the physical prototype is solidified, designers can finalize the placement using the built-in device placer. At this point, designers are ready to connect the devices either manually or using an automated router such as the Titan Shape-Based Router (SBR).

Titan AVP works directly on the Titan Layout Editor (LE) instances and supports PCells/PyCells. The prototype layout creation is schematic driven with the initial placement and hierarchy preserved as in the schematic. The editing of the generated layout is assisted with hierarchical cross-probing and a bird's eye view.

Titan AVP supports flattening of instances for compact layout creation. The checking and updating of the layout is done hierarchically, even with a modified layout hierarchy, giving designers complete flexibility to create a full-custom layout.

The prototype layout created with Titan AVP can be used to generate floorplan constraints for Titan ADX, Magma's circuit optimization solution. Titan ADX simultaneously works on the circuit and floorplan constraints to optimize for the layout area. The circuit sizes obtained fit into a very compact layout. Physically aware circuit sizing is a significant breakthrough in analog design and minimizes the time and effort required by the layout engineers to create a compact layout.

Titan Device Placer is a powerful constraint-based auto placement tool for various placement styles including area, row and stack. This unique placement engine can support concurrent placement of constrained objects, including blocks, standard cells, devices and pins. A consolidated constraint management system manages constraints for placement styles and objects with intuitive GUI and/or flexible Tcl commands. The same constraint management system is also used by other Titan applications including



schematic, floorplanning and routing. This provides an extremely efficient implementation environment for mixed-signal design.

Titan AVP and Titan SBR can be used together to effectively incorporate last-minute schematic changes within a day.

Technology Features

Prototype Layout Creation

- Hierarchical layout generation with flattening capabilities based on real PDK
- Prototype placement mirrors placement in schematic initialization
- Quick manual placement – PowerPoint style grouping/ungrouping of objects
- Simplifies entry of placement constraints including symmetry, alignment and spacing
- Supports device modules
- Ability to add guard rings on groups
- Interactive placement and creation of a generic floorplans
- Hierarchical cross-probing between schematic and layout
- Virtuoso data compatibility using translators
- Works on Titan LE instances and supports PCells/PyCells

Automated Device Placement

- Fast and high capacity congestion-aware global/detail placement
- Flexible and rich placement constraints
 - Alignment/symmetrical/confinement/orientation/range/pre-placement
 - Ordering/grouping/clustering
 - Row/column with direction/type/grid/orientation constraints

- Region confinement
- I/O grid/siding/pitching constraints
- Instance type and spacing rules
- Intuitive and easy-to-use constraint manager
- Rule-driven automatic placement
 - Automatic device chaining
 - Device row planning
 - Dynamic device abutment during placement
- Interactive placement
- Auto-stack rule extraction
 - Supports hierarchical stack rules

Placement-Aware Layout Update

- Hierarchical update of layout/floorplan based on changes in schematic
- Complete control of hierarchy during update
- Maintains relative placement, symmetry, alignment and spacing

Layout-Aware Simulation Flow

- Extraction of proximity parameters from partial layout
- Netlisting of extracted parameters from the prototype layout
- Complete reuse of schematic testbench for layout-aware simulation
- Back annotation of extracted proximity parameters onto schematic
- Parasitic net cap estimation based on placement

Integration with Titan ADX

- Relative placement constraints written for circuit sizing
- Automatic update of placement with the optimized circuit sizes
- Net route equations for parasitic cap estimation during optimization

Supported Platforms

- Linux 32 and 64 bit

MAGMA DESIGN AUTOMATION

Titan™ AVP



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