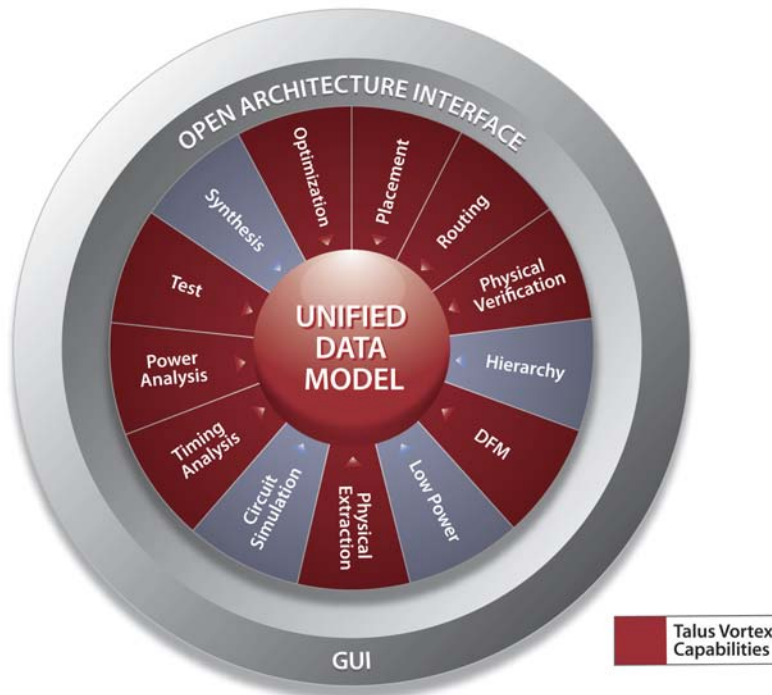


Talus[®] Vortex

Talus Vortex is the physical design environment of choice for engineers creating ICs at advanced geometries, for complex integrated systems, or designs where power management is important. It dramatically improves the productivity of designers by providing reference flows and a flexible, integrated infrastructure based on Magma's unified data model. With Talus Vortex, designers can tackle new technologies and achieve design closure in a predictable fashion.

- Talus COre™ technology, a fully timing-driven incremental routing and optimization engine, delivers predictable area and timing results, to within 5 percent between placed gates and final layout.
- Integrated placement and clock tree synthesis (CTS) improves maximum frequency on low-power designs by up to 25 percent.
- Robust multi-mode/multi-corner (MMMC) low-power clock tree synthesis reduces the amount of runtime and area required to close timing across multiple corners.
- Provides the capacity to handle over 3.5 million placeable instances flat, with full-flow MMMC and multi-threading technology.
- Proven design support for major silicon vendors and foundries up to and including 28-nanometer (nm).
- Talus® Flow Manager™ and Talus® Visual Volcano™ allow rapid deployment of an RTL-to-GDSII flow and help communication between distributed teams by displaying design data through HTML-based reporting.
- Full-flow support for composite current source (CCS) delay models for timing optimization reduces pessimism and increases accuracy for 28-nm designs.
- Integrated design flow, single executable, common analysis engines and a unified data model enhance productivity, provide ease of use, eliminate unnecessary file transfers and ensure continuous correlation to final implementation.



The challenges faced by today's designers require an integrated solution that produces ICs that are built correct by construction. From the beginning, Magma has offered a single executable, unified datamodel solution for IC design that addresses these challenges. Concurrent optimization during placement was the first breakthrough delivered by this solution. The new Talus Concurrent Optimizing Routing Engine (COre) technology enables optimization during routing, resulting in faster design closure and better timing performance. Unlike other approaches, Talus Vortex delivers a level of design speed and efficiency that is ideal for 28-nm designs and for designers creating big chips. It is also well-suited for customer designs that target applications such as tablets, smartphones and networking and embedded devices that require bigger and more complex chips that also must be designed for low power.

Talus[®] Vortex

The Talus Vortex implementation system provides a fully integrated netlist-to-GDSII flow for high-performance, high-complexity, low-power nanometer designs that includes optimization, placement, routing, useful skew clock generation, floorplanning and power planning, incremental RC extraction and a single incremental timing analysis engine. Built on Magma's unified data model and employing a silicon validated nanometer strength-based delay model, Talus Vortex sets a new standard for capacity, runtime and performance.

In conjunction with the comprehensive low-power design capabilities of Talus Power Pro, Talus Vortex provides significant power reductions without sacrificing timing and area.

Talus Vortex delivers the fastest timing closure on the largest and most complex semiconductor designs. Talus Vortex 1.1 utilizes the new Talus COre technology, which leverages Magma's unified data model to perform timing optimization concurrently during routing, providing faster overall design closure with better performance and predictability. This greatly enhances the designer's ability to achieve optimal results across a wide variety of designs – while minimizing the need for user intervention. Unlike existing routing systems that perform optimization sequentially before and after place and route, and which focus only on layout-oriented routing factors such as design for manufacturability (DFM) or design rule checking (DRC), Talus focuses concurrently on timing and layout-driven metrics during routing.

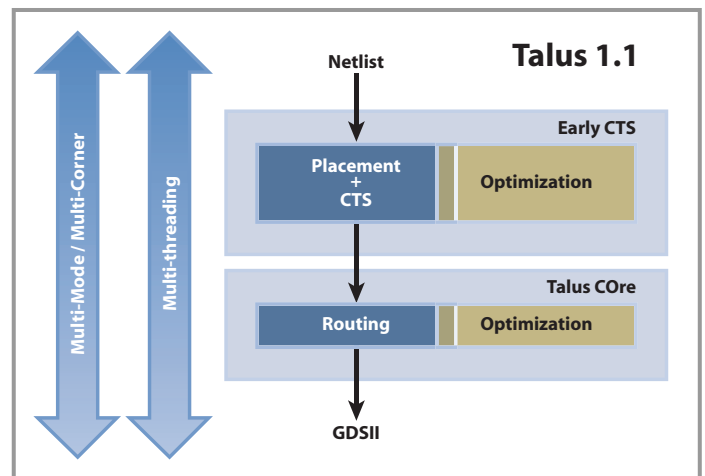
To address the needs of today's complicated systems on a chip, Talus Vortex's netlist-to-GDSII flow is fully multi-mode and multi-corner enabled. All design operating modes and corners are defined at the start of the flow, and the implementation system concurrently analyzes and optimizes across all combinations to produce the best results while managing the runtime and memory overhead with the MMMC Accelerator. This produces a better design and saves costly iterations with sign-off MMMC.

In addition to providing the fastest turnaround on large designs, Talus 1.1 introduces the Talus Flow Manager with an out-of-the-box design flow template. Engineers can easily tune the reference flow for their specific application. Talus Flow Manager also introduces a new visual analysis environment, Talus Visual Volcano, that integrates and presents all design and analysis data via a common display.

Talus COre Technology

The heart of the improvements in Talus Vortex 1.1 is its COre technology. At advanced geometries, complex routing resistance effects, increased via resistance and crosstalk can create a large disconnect between placed gates and final routing timing. Dealing with optimization and routing sequentially results in

a suboptimal solution with unpredictable results. Traditional solutions must optimize the design after routing to get the necessary accuracy, increasing runtimes. Talus COre applies the full scope of timing optimization incrementally during routing. Every aspect of the routing algorithms – from topology generation to layer assignment, track assignment and DRC cleanup – is timing and crosstalk aware. This allows the design to converge faster and eliminate post-route timing surprises. Talus COre is coupled with Talus' SDF-based optimization to remove the need for manual engineering change orders (ECOs) to close timing. Talus COre considers all modes and corners and setup and hold limit violations concurrently when optimizing the design.



Featuring an integrated physical design flow, Talus COre Technology and early clock tree synthesis, Talus 1.1 delivers optimal results out of the box.

The addition of the Talus COre technology allows Talus 1.1 to deliver optimal quality of results out of the box on advanced process node design challenges. It has already been used to complete production designs where it provided 5 times faster runtime over competitive solutions. In customer testing on 40-nm designs ranging from 2 million to 4 million gates, with frequencies from 400 MHz to 800 MHz, Talus 1.1 produced 75 percent better timing with 10 percent fewer vias than the competitive results.

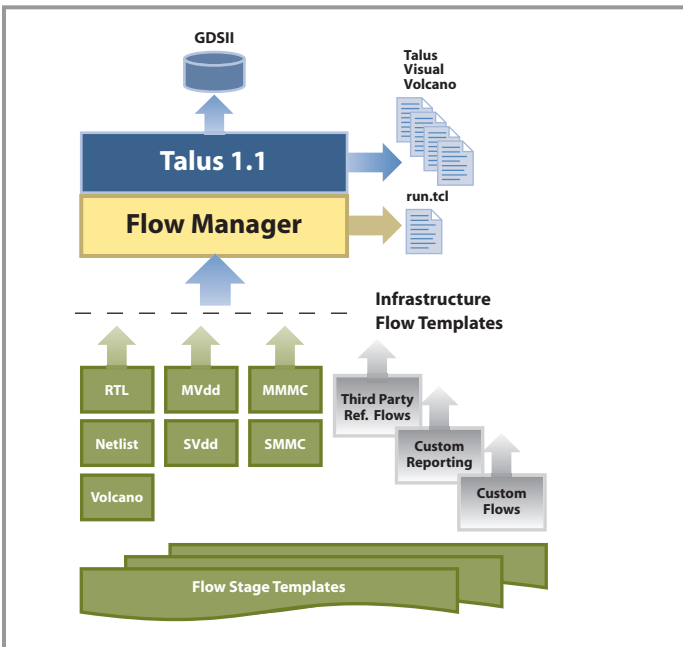
The Talus COre Technology is fully integrated into the next generation router included in Talus Vortex. It incorporates speed and rule improvements to deliver fast, DRC-clean routing. It can perform top-level (hierarchical) as well as standard-cell routing. A built-in polygon-based DRC engine provides clean routing and immediate feedback for advanced interactive routing. Talus Vortex fully supports 45-nm and 28-nm design rules from major silicon vendors and foundries, including complex spacing rules, common run-length rules, stacked-viarsules and dense end-of-line rules. Talus Vortex

automatically addresses complex antenna rules as well as other process-specific manufacturing requirements such as minimum area rules for vias, metal slotting and timing-driven metal fill. The integrated engines operating on the single data model allow for fast and accurate timing-driven wire spacing, metal fill for both grounded and floating metal, and native redundant via insertion.

Talus Flow Manager and Talus Visual Volcano

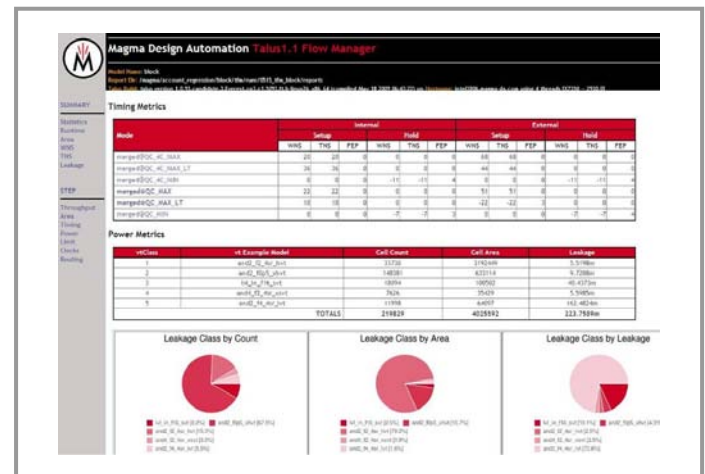
The Talus Flow Manager provides an out-of-the-box RTL-to-GDSII design flow tuned to deliver optimal results. Designers can easily customize the reference flow and tailor it to their own needs, developing specific flows for various projects or applications. Additional reference flows include templates for the implementation of multiple-voltage (MVdd), MMMC designs, as well as low-power and high-performance designs. Ease of use and cost of adoption is dramatically improved through the use of these pre-qualified flows for small design teams or large, geographically distributed groups.

designers time and improves efficiency by eliminating the need for tedious analysis of log files and textual reports. Block designers, chip integrators or design managers can now all communicate with a common format and make better design decisions as a team.



The Talus Flow Manager allows designers to customize reference flows.

The Talus Flow Manager includes the new Talus Visual Volcano, a new technology designed to help designers make better decisions faster. The Talus Visual Volcano analysis environment offers an integrated information display that allows an engineer to quickly track many parameters of the design, including runtimes, timing, power and area. MMMC design management is made easier by simplifying the control over active versus reported scenarios, and displaying results for all scenarios concurrently. By consolidating this data into HTML charts and graphs, the Talus Visual Volcano saves



The Talus Visual Volcano eliminates the need for tedious analysis of log files and textual reports.

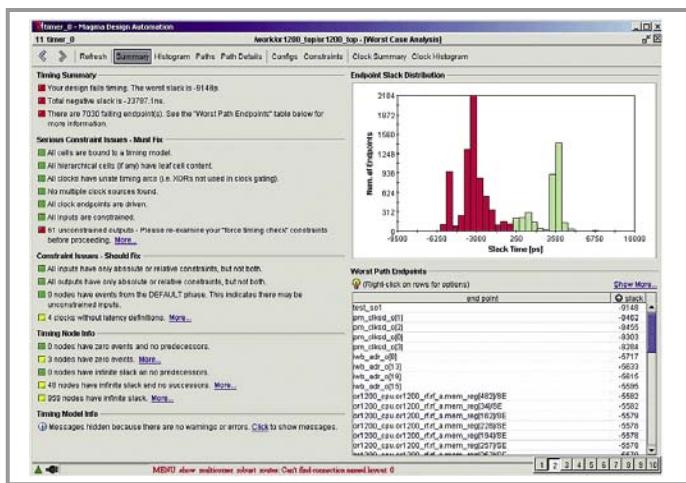
Early Clock Tree Synthesis

One of the biggest problems with IC design is lack of a predictable, smooth flow to close timing and minimize power. Talus Vortex 1.1 integrates the creation of a clock tree with physical placement and synthesis. This removes the expensive iterations required to re-optimize the design after clock tree synthesis, and allows concurrent placement, clockgate cloning and data-path optimization to deliver the optimal solution.

The complex clock trees on today's advanced low-power designs require this type of approach. On mobile and wireless designs, early clock tree synthesis can help boost the maximum frequency by up to 25 percent by optimizing the complex clock-gate-enable paths more efficiently.

Robust MMMC Clock Tree Synthesis

MMMC clock tree synthesis is fully integrated to ensure that the clocks meet both timing and physical goals and also optimize for power with the Talus Power Pro option. Talus Vortex takes advantage of advanced techniques such as optimal clock-gate placement and cloning and un-cloning for better load distribution. It also leverages sophisticated clock algorithms that minimize skew while achieving timing requirements and maintaining design robustness under process variations and environmental differences. With the unique clock-tree visualization interface, users can browse, analyze and visualize the clock tree with ease.



Talus Vortex's unique clock viewer allows users to browse, analyze and visualize the clock tree with ease.

Industry's Highest Capacity through Multithreading and MMMC Accelerator

Talus Vortex consistently delivers the industry's highest capacity. This allows users to create larger blocks, saving resources and time by eliminating the need to partition a design into many small blocks. Depending on the complexity of the design, blocks from 1 million to over 3.5 million instances can be implemented flat with Talus Vortex 1.1. This capacity is enabled through Magma's integrated platform and the single executable of the Talus Vortex system. Traditional solutions require extensive file transfers and translations between different steps of the implementation process resulting in longer turnaround times.

The full place-and-route flow is also multithreaded and able to both analyze and optimize for multiple modes and corners. Talus Vortex's MMMC Accelerator provides industry-leading runtime and memory management for today's complex designs. The use model is simple: supply Talus Vortex all of the mode/corner combinations for the design at the start of the flow, and run. The MMMC Accelerator is able to intelligently

and efficiently manage the scenarios throughout the design flow to ensure the best quality of results in the shortest amount of runtime.

Built-in Low-Power Design and Optimization

Talus Vortex, with Talus Power Pro as an option, provides an integrated power optimization flow, reducing power up to 20 percent over conventional standalone implementation tools while also delivering high performance. This option can enable advanced, low-power designs including voltage island support, automatic MTCMOS switch insertion and dynamic voltage and frequency scaling (DVFS). It is the only commercial platform available that supports both the Unified Power Format (UPF) and Common Power Format (CPF). Power optimization capabilities deliver lower dynamic power consumption than conventional synthesis. Talus Vortex's MMMC low-power clock tree synthesis minimizes the dynamic and static power from clock tree networks. Only optimal cell sizes are used to drive known loads, avoiding unnecessary power dissipation by cells. Balancing input slews to cells through optimal sizing is used to reduce total switching power. Additional power optimization capabilities such as multi-Vt library-based optimization, DFT-aware automatic clock gating, use of integrated clock gating cells in the standard-cell library, detection of synchronously enabled registers and hierarchical insertion of clock gating logic minimize power and improve testability. This automated method significantly reduces design closure time without sacrificing performance.

Advanced-Node Designs

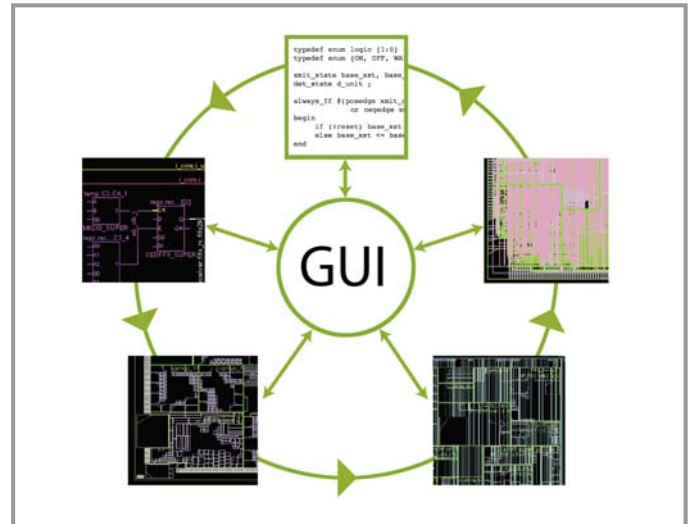
Talus Vortex is the platform of choice for advanced-node designs, and is tapeout-proven at 28 nm. Full-flow support for CCS timing models provides the needed accuracy for 28-nm designs. Next generation routing and the Talus COre technology deliver superior capacity and quality of results. The MMMC Accelerator allows design size to increase without sacrificing the number of modes or corners used in implementation. Talus Vortex with Talus qDRC can invoke the Quartz™ DRC engine to implement timing driven, sign-off quality pattern-based fill that is required to achieve yield targets at advanced process nodes including 45 nm and 28 nm.

Predictability Improves Productivity

With the automated flow of Talus Design and Talus Vortex, implementation is no longer the bottleneck in the design process. System-level designers can rapidly assess the impact of alternate system architectures on physical metrics such as area, performance, power, routability, testability, manufacturability and yield. Any late-arriving specification, RTL, netlist or constraint changes can be easily accommodated without affecting the schedule or the productivity of the engineering team.

Powerful GUI Speeds Design Debug and Exploration

Using the powerful Talus Vortex visualization tool, designers can browse the logical hierarchy and guide partitioning decisions needed for floorplanning. Connectivity-driven visualizations such as fly-lines and clock-domain distribution provide valuable architecture and constraint improvement information. Slack-based timing histograms of critical paths in the built-in timing visualizer allow designers to quickly locate timing problems through direct cross-probing of RTL (with Talus Design), schematic, floorplan or layout. Such analysis readily leads to identification of missing constraints or exceptions such as false paths or multi-cycle paths. Detailed power reports and maps provide power consumption and distribution information early in the design flow, saving back-end packaging and design re-spin costs.



Cross-probing accelerates quality improvement.

TECHNOLOGY FEATURES:

Ease of Use

- Library processing
- Integrated datamodel and single timer/extractor
- Query DB, GUI, Tcl, Reporting
- RC extraction for implementation
- Cross-probing between layout, netlist, schematic, timing GUI and RTL
- Built-in reference flow (Talus Flow Manager) and visualization (Talus Visual Volcano)

Timing Closure and Core Technology

- Netlist-to-GDSII flow (RTL-to-GDSII flow with addition of Talus Design)
- Strength-based physical synthesis
- Early clock tree synthesis during placement
- Signal integrity analysis/optimizations (crosstalk noise, crosstalk delay)
- Static timing analysis and optimization with OCV, common point pessimism removal (CPPR) and crosstalk
- MMMC analysis/optimizations with OCV and crosstalk
- Robust MMMC clock tree synthesis
- Early crosstalk avoidance flow
- Talus Core Technology - Concurrent Routing and Optimization Engine
- Surgical wire optimization for timing and DRCs
- Rapid timing closure with SDF back annotation
- Concurrent MMMC aware setup/hold/limit/DRC optimization
- Full-flow multi-threading (with Talus MCPPU)

Large Designs

- Over 3.5-million-instance flat capacity
- MMMC Accelerator
- Full-flow multithreading (with Talus MCPPU)

Advanced Nodes

- 40- and 28-nm routing
- Full-flow CCS optimization and analysis
- Wire spreading and widening (basic or CAA)
- Recommended end-of-line extensions
- Redundant via insertion
- Cell yield optimization
- DFM soft rules
- Timing-driven metal fill [density or chemical-mechanical polishing (CMP)]
- Automated SPICE delay and crosstalk noise correlation
- Emulated metal-fill extraction

Low Power

- Embedded static power analysis
- Multi-VT leakage optimization
- MVdd and UPF/CPF support (with Talus Power Pro)

Advanced Placement and Optimization Features

- Early useful-skew estimation and implementation
- Advanced timing visualization
- Incremental extraction, timing and noise
- Comprehensive congestion analysis
- Scan chain reordering
- Multi-height cell placement with power/ground rail sharing

Advanced Clock Tree Features

- Useful/zero skew
- Low-power clock tree implementation using clock cloning/un-cloning and clock gates
- Inter-clock skew minimization
- Multiple clock domains
- Automatic gated-clock checks
- Clock tree viewer
- Support for complex non-default rules and clock shielding

Advanced Routing Features

- Virtual gridless router
- Interactive bus routing
- Complete ECO support
- 28-nm design and manufacturability rules
- Built-in polygon-based DRC engine
- DFM-aware routing
- Crosstalk and timing driven

Crosstalk Noise Analysis

- DC and AC noise thresholds
- Accounts for multiple aggressors
- Timing window-based filtering
- Capacitance-based filtering
- Logical correlation filtering

Crosstalk Delay Analysis

- Timing window-based filtering
- Capacitance-based filtering
- Logical correlation filtering
- Slew-based crosstalk delay prevention
- Automatic timing window convergence

Inputs

- DEF (floorplan), Verilog (netlist), .lib, SDC, SPEF, LEF, GDSII, UPF, CPF, Volcano™ (Magma format)

Outputs

- DEF (floorplan), Verilog (netlist), .lib, SDC, SPEF/DSPF, LEF, GDSII, Volcano (Magma format), UPF, HTML

Platforms

- Linux, Sun Solaris

MAGMA DESIGN AUTOMATION

Talus® Vortex



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