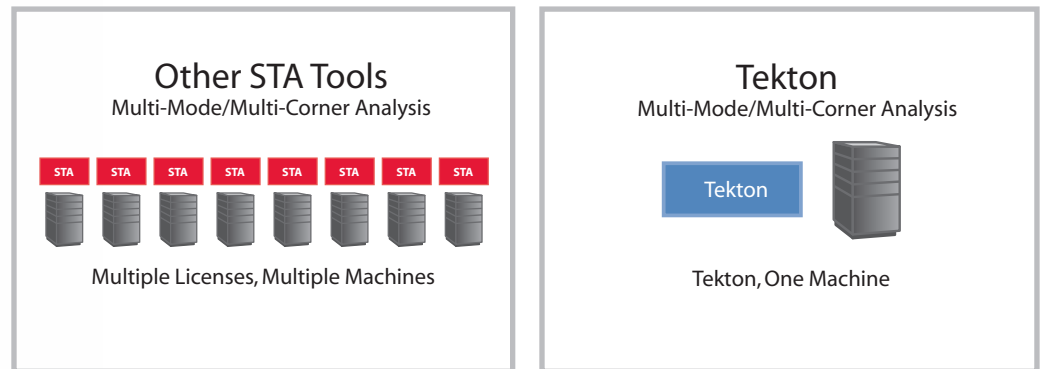


Tekton™

- Performs extremely fast and accurate multi-scenario timing analysis for large designs and blocks on a single CPU machine. Its multi-threaded architecture provides scalable performance for designs of any size.
- Supports all SDC versions, Magma Tcl and scripts from existing STA flows. Enables users to view timing reports in Magma's configurable format, or in formats that they are already familiar with.
- Provides both crosstalk analysis and AOCV for sign-off quality timing analysis, which are required for accurate analysis at 40 nm, 28 nm and below.
- Offers an embedded SPICE engine to analyze critical paths with minimal overhead and full SPICE accuracy when needed.
- Operates with QCP™, Magma's high-speed, high-capacity extraction tool, in a single session, shortening ECO cycles.

Tekton is a next-generation STA tool. It provides groundbreaking multi-mode/multi-corner performance on single CPU machines, delivering timing updates for tens of millions of instances in minutes. It provides full support for crosstalk analysis and AOCV and offers an embedded SPICE engine when extremely high accuracy is required.



Timing analysis has become a key bottleneck for many chip design teams. With design sizes often exceeding 10 million gates and requiring analysis across many operating scenarios, the impact on schedules is severe. Design teams have been forced to address the limitations of current static timing analysis (STA) solutions by either investing in additional hardware and STA licenses or by cutting corners and restricting the number of scenarios that are analyzed. These approaches are both expensive and cannot scale. What design teams need is a fast, high capacity timing analysis solution that can provide sign-off quality timing analysis on standard hardware in minutes, not hours or days.

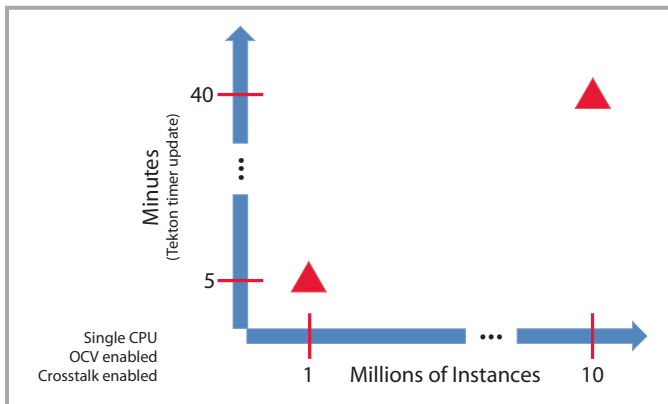
Tekton was architected specifically to address the requirements of 40 nanometer (nm), 28 nm and beyond. Using Tekton, design teams can run very large designs with multiple scenarios on a single CPU machine in minutes. Tekton provides an order-of-magnitude performance improvement on a single CPU machine and is fully multi-threaded to deliver even faster performance on multi-CPU machines. Near-linear performance scaling across multiple CPUs enables Tekton to scale well into the future for designs with hundreds of millions of gates and beyond.

Tekton raises the bar on accuracy by including an embedded SPICE engine. This integrated engine enables design teams to combine advanced on-chip variation (AOCV) with path-based analysis and SPICE without significant runtime increases. Tekton has been architected to be the next-generation timing analysis platform, offering the most accurate timing analysis engine in the industry.

Tekton™

Fast, High-Capacity STA in Minutes

Tekton delivers breakthrough speed and capacity to address the design sizes and complexities of 40 nm, 28 nm and beyond. Based on a new architecture, Tekton provides best-in-class single-CPU performance and near-linear scaling on multi-CPU machines up to 24 CPUs. With this architecture, Tekton has the capability to complete a full timing analysis run, with OCV and crosstalk analysis enabled, on 40-million-gate designs in under an hour on a single CPU. The single-CPU performance alone sets it apart from other industry STA tools.



Tekton provides sign-off quality timing analysis on standard hardware in minutes.

Compatible with Existing STA Flows

Tekton provides an easy-to-use STA environment. In addition to supporting all SDC versions and Magma Tcl, Tekton also supports scripts from existing STA flows. It provides the user the flexibility to view timing reports in Magma's configurable format, or in formats that chip design teams are already familiar with.

Single-Machine Multi-Mode/Multi-Corner Analysis Scales with Increasing Scenarios

Today's complex designs require timing analysis across a large number of timing modes and PVT corners. A key capability of Tekton is that it offers the capability of running all of the

timing scenarios on a single CPU, or optionally, on multiple-CPU's. Unlike existing solutions that require a distributed approach, with one machine and one license required for each scenario, Tekton can quickly run a large number of scenarios on a single machine. To accomplish this, the designer uses a single STA script that imports all the timing SDCs, libraries and SPEF files into Tekton running on a single machine.

AOCV Minimizes the Impact of Timing Margins

Designers have been adding timing margins to their designs for years. As process geometries continue to shrink, the margins have made timing closure more difficult, lengthening schedules significantly. As design teams approach 28 nm, AOCV is being viewed as a methodology that can potentially reduce the pessimism in OCV. Tekton fully supports AOCV. Designers are able to derate clock or data-paths by reading in derating tables or via command line input.

Integrated SPICE Engine for Analyzing Critical Paths

Implementing engineering change orders (ECOs) as fast as possible is critical to achieving timing closure on schedule. Tekton provides very fast timing iterations, enabling fast ECO cycles. As design teams approach the last group of timing violations, their design is often in a state where timing or area disturbances can increase die size and/or lengthen the schedule. Tekton's embedded SPICE engine allows users to analyze critical paths with minimal overhead and full SPICE accuracy.

Tight Integration of STA and Extraction Engines

The separation of implementation and analysis tools results in decreased accuracy at 28 nm. Tightening the gaps between place-and-route, extraction and STA provides the accuracy required for faster timing closure. Tekton and the QCP extraction tool are standalone tools that are based on the same architecture. With this common architecture, designers can reduce STA runtime through the use of QCP-generated binary SPEF. Alternatively, designers can extract parasitics using QCP directly from a Magma Volcano™ during a Tekton timing session.

TECHNOLOGY FEATURES:

- Timing analysis of the largest designs in minutes
- Multi-mode/multi-corner timing analysis on one or more CPUs
- Integrated SPICE engine for critical path analysis
- Very fast, accurate what-if analysis
- AOCV for reducing OCV pessimism
- Tight integration of timing and extraction

Inputs

- Verilog
- Liberty format (.lib)
- Interface logic modules (ILM)
- Extracted timing models (ETM)
- Volcano (Magma format)
- SDF, SPEF, Magma binary SPEF
- STA constraint files (SDC, m-Tcl, third party)

Outputs

- Volcano (Magma format)
- Verilog netlist
- SPEF, SDF
- Timing reports



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