

MUSIC India 2010 Agenda

Start	Papers/Activity	Company
9:30	Welcome	
9:45	A Solution to Power Optimization using the Magma UPF Flow	Nokia
10:10	Evaluation of SiliconSmart CCS Library Modeling for Accurate and IR-Drop-Aware Timing Analysis	SanDisk
10:30	Tea Break	
10:45	Optimal Design Methods for Multi-Voltage Domain, Multimillion-Gate SoCs using Talus GRX, MMMC and CITL	Texas Instruments
11:15	“Honey, I Shrunk the TAT!!” – Implementation of an Extremely Schedule-Critical 45 nm, Multimillion SoC using Talus 1.1	Qualcomm
11:50	Early and Efficient Decap and Automatic Power Metal Fill Insertion Using Talus	Texas Instruments
12:15	Keynote: "Electronic Ocean," Rajeev Madhavan, CEO Magma	
13:00	Lunch	
13:45	FineSim Simulation Verification and Performance for Mixed-Signal/Analog Blocks in Complex SoC Designs	Conexant
14:10	A Convergent Routing Methodology for High-Performance Designs	Texas Instruments
14:45	Predictable Timing Closure for Hierarchical Designs using the Talus Flow Manager	Open-Silicon Research
15:15	Tea Break	
15:30	Talus Vortex 1.1's Enhanced Router for 28 nm	Qualcomm
16:00	Case Study of Efficient Design Closure Methodologies in a Timing-Critical and Highly Congested Multi-Core, Complex SoC	Texas Instruments
16:30	Minimum-Pulse-Width Measurement Methodology	Qualcomm
17:00	Closing Remarks, Prize Distribution	